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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,033	10/23/2003	Dong-Gyu Kim	9649-288DVCT	6453

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,033	KIM, DONG-GYU	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-30* is/are rejected.

7)☒ Claim(s) *31-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/777,506.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *102303*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Shin et al., US Patent No. 5,737,049.

Shin anticipates a method for manufacturing a thin film transistor array panel used for a liquid crystal display, comprising:

in fig. 3, forming a gate line 40, gate line a.k.a. scanning line col. 6, lines 57-65, and, in fig. 2A, a gate electrode 21 on a substrate 1;

in fig. 2B, forming an insulating layer 24 on the gate line and on the gate electrode;

forming a semiconductor layer 26, 27 on the insulating layer;

in fig. 3, forming a data line 50, data line a.k.a. signal line, col. 6, lines 57-65, in fig. 2, a source electrode 29 and a drain electrode 30 on the substrate,

in fig. 2E, forming a passivation film 31 on the semiconductor layer, the data line, the source electrode and the drain electrode, the passivation film exposing a portion of the drain electrode 32-1 and a portion of the semiconductor layer 27", 33-1,

removing the exposed portion 27' of the semiconductor layer; and

in fig. 2F, forming a pixel electrode 33 that contacts the exposed portion of the drain electrode, col. 4, line 59 - col. 6, line 53;

limitations from claim 23, the method of claim 22, wherein the passivation film comprises opaque material, silicon nitride, col. 5, lines 44-57;

limitations from claim 24, the method of claim 22, in fig. 2E, wherein a portion of the passivation film is located on the gate line and the gate electrode;

limitations from claim 25, the method of claim 24, in fig. 2E, wherein the removal of the exposed portion of the semiconductor layer exposes a portion of the insulating layer 24, and further comprising: 32-2 removing the exposed portion of the insulating layer, col.6, lines 17 - 29;

limitations from claim 26, the method of claim 25, further comprising:

in figs. 2E, 3, forming a connection portion that overlaps a part of the gate line on the insulating layer, 30;

limitations from claim 27, the method of claim 26, in fig. 2F, wherein a part of the connection portion 30 is exposed outside the passivation film 31 and is connected to the pixel electrode 33.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin.

Shin teaches a method for manufacturing a thin film transistor array panel used for a liquid crystal display, comprising:

in fig. 2A, depositing a first conductive layer on a substrate 1;

patterning the first conductive layer to form, in fig. 3, a gate line 40, in fig. 2A, and a gate electrode 21;

in fig. 2B, depositing an insulating layer 24 on the gate line and on the gate electrode, depositing a semiconductor layer 25 on the insulating layer;

in fig. 2C, depositing a second conductive layer on the semiconductor layer;

patterning the second conductive layer to for, in fig. 3, a data line 50, col. 6, lines 56-65, in fig. 2C, a source electrode 29, and a drain electrode 30;

in fig. 2E, depositing a passivation layer 31 on the semiconductor layer, the drain electrode, the source electrode and the data line;

patterning the passivation layer to expose a portion 32-2 of the semiconductor layer 27", a portion of the data line 30, and a portion of the drain electrode 30;

removing the exposed portion of the semiconductor layer 27" to expose a portion of the

insulating layer 24,

removing the exposed portion of the insulating layer 24, bottom portion of 32-2; and in fig. 2F, forming a pixel electrode 33 that contacts the exposed portion of the drain electrode, col. 4, line 59 - col. 6, line 53;

limitations from claim 29, the method of claim 28, further comprising:

in fig. 2E, forming transparent conductive pads 33 that cover the exposed portions and the data line 33, ITO, col. 6, lines 35-48;

limitations from claim 30, the method of claim 28, in fig. 2A, wherein the first conductive layer comprises a portion of the gate line, an upper layer 22 and a lower layer 21 of different materials, col. 5, lines 8-11.

Although Shin does not explicitly display it, the gate line (scanning line) of fig. 3, will have to be connected through a contact as the device would be useless without a way to deliver a potential to the gate 21. In order to form the contact, since the gate electrode is at the bottom of the layers, the practitioner would have to follow the steps of:

limitations from claim 33, the method of claim 32, further comprising:

removing the exposed portion of the upper layer 22, at least a few atomic layers;

limitations from claim 34, the method of claim 33, wherein the patterning of the second conductive 30 layer exposes a portion of the n+ amorphous silicon layer 25, and further comprising:

removing the exposed portion of the n+ amorphous silicon layer after patterning then second conductive layer;

limitations from claim 29, the method of claim 28, further comprising:

in fig. 2E, forming transparent conductive pads 33 that cover the exposed portions and the gate line 33, ITO, col. 6, lines 35-48;

Allowable Subject Matter

Claims 31-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

18 January 2005
WB